REMARKS

Favorable consideration of this application as presented herein is requested. Claims 4, 5, 7 and 8 are pending in this application for reconsideration following amendment. No new matter has been added. In the January 2, 2002 Office Action, the Examiner rejected Claims 4, 5, 7 and 8 under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 5,063,359 to Leonowich ("the Leonowich Patent") in view of U.S. Patent No. 6,111,473 to Homberg ("the Homberg Patent") and U.S. Patent No. 5,285,168 to Tomatsu ("the Tomatsu Patent").

The Examiner also rejected Claims 4, 5, 7 and 8 under the judicially created doctrine of obviousness-type double patenting over all claims of U.S. Patent No. 6,242,980 to Tsukagoshi et al. ("the Tsukagoshi Patent") in view of the Leonowich Patent.

Finally the Examiner objected to the drawings under 37 C.F.R. 1.83(a) for failure to show every feature of the invention specified in the claims.

Claim Rejections Under 35 U.S.C. § 103(a)

First, with respect to the rejections to Claims 4, 5, 7 and 8 under 35 U.S.C. § 103(a), Applicants have amended Claims 7 and 8 to specify that unlike in the Tomatsu Patent, the first signal (disclosed as XT) from a terminal of an oscillator is input into both differential amplifier circuits (disclosed as D1 and D2) and the second signal (disclosed as XTN) from a second terminal of an oscillator is input into both differential amplifier circuits (disclosed as D1 and D2). That is, as disclosed, the gate of MOS transistor 5 of D2 and the gate of MOS transistor 1 of D1 receive the first signal XT from the oscillator. And, as discussed, the gate of MOS transistor 6 of

D2 and the gate of MOS transistor 2 of D1 receive the second signal XTN from the oscillator. This is different from the Tomatsu Patent where Q 21, Q 22, Q 26 and Q 27 receive gate signals from MOSFETS of the input stage amplifier. In other words, each signal from an oscillator is separately amplified before the difference is reflected in the output.

Referring to FIG.1 of the present application, the output signal at the output of the CMOS inverter X1 has an oscillating component riding on an operating point potential. The operating point potential can fluctuate due to, for example, factors relating to semiconductor manufacturing processes, or to fluctuation of power supply potentials V_{DD} and V_{SS} caused by the oscillation at the output of the inverter. The fluctuations in the operating point potential affect, in turn, the duty ratio of the alternating signal at the output of the CMOS inverter. Inasmuch as the CMOS inverter X2 has a predetermined threshold, fluctuations in the duty ratio of the output signal of the CMOS inverter X1 caused by fluctuations in the operating point potential of the output signal make it difficult to maintain a predetermined duty ratio for the output signal from the CMOS inverter X2. The specific signal treatment and differential amplifier configuration is directed to eliminating these problems to output a signal where the duty ratio is unchanged from that of first and second signals from an oscillator and the operating point of the output signal is at an intermediate point between the power supply potentials regardless of the operating point of the signals from the oscillator and fluctuation in the operating points. Tomatsu is not directed to solving the problem of operating point fluctuations during amplification of oscillating signals or to the problems that fluctuations cause in the duty ratio.

As mentioned by the Examiner, the Leonowich Patent fails to describe the specifics of the differential amplifier as claimed. There is no teaching to modify or replace the differential amplifier of Leonowich. Leonowich does not disclose combining differential amplification outputs as recited in Claim 7 or an output buffer as recited in Claim 8. Further, as specified by the claim amendment, the signal treatment as well as the specific function of the differential amplifiers is not obvious from Tomatsu. If, for the purposes of argument only, one were to seek lower power consumption by looking to Tomatsu, the result would necessarily require all of the circuit in Tomatsu, not just part of it. The rejection is based upon picking and choosing just parts of the Tomatsu circuit for driving a low impedance load and combining them with the oscillator of Leonowich, despite the fact that Tomatsu does not contemplate an oscillator input. This is impermissible hindsight of picking and choosing circuit elements to arrive at the claimed invention using the Applicant's own disclosure as a roadmap. Thus, Claims 7 and 8 are not met by Leonowich or Tomatsu, taken alone or considered in combination.

Claims 4 and 5 are dependent on Claim 8, and therefore, contain all the limitations of that claim. Thus, Claims 4 and 5 are patentable for the reasons set forth with respect to Claim 8. Since the Leonowich and Tomatsu Patents do not render Claims 4, 5, 7 and 8 unpatentable alone or in combination with the other prior art of record, Applicants respectfully submit that the rejections thereof be withdrawn by the Examiner.

Double Patenting Rejection

With respect to the rejections of Claims 4, 5, 7 and 8 based upon the judicially created doctrine of obviousness-type double patenting over all claims of the Tsukagoshi Patent in view of the Leonowich Patent, Applicants respectfully submit the new enclosed Terminal Disclaimer. Nippon Precision Circuits Inc. is the current owner of the present application as well as the owner of the parent U.S. Patent No. 6,242,980 B1, of the present application. The assignment of the '980 patent was recorded on 01-22-1999 at Reel No. 9728 and Frame No. 0485.

Drawings

The drawings were objected to under 37 C.F.R. 1.83(a) for failure to show every feature of the invention specified in the claims. Accordingly amendments to the drawings (FIGS. 2, 4, 6, 9A, 9B and 9C) are requested, with changes in red, to show the placement of the oscillator (OSC) at the input of the specific differential amplifier arrangement. Filed concurrently is a "Request to for Approval of Drawing Corrections".

These drawings are supported in the specification, more specifically on page 4, lines 12 to 24 as well as page 9, lines 10 to 20.

Applicants respectfully submit that this application is in condition for allowance and request that a timely Notice of Allowance be issued in this case.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Respectfully submitted,

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Dated: June 28, 2002
New York, New York

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please note that the use of "[]" indicates that the phrase is deleted and use of "__" indicates that the phrase is added.

In the claims:

Claims 7 and 8 have been amended as follows:

7. (Amended) An oscillation circuit, comprising:

a first differential amplifier circuit including a differential input portion comprising a pair of MOS transistors of a first conductivity type;

a second differential amplifier circuit including a differential input portion comprising a pair of MOS transistors of a second conductivity type; and

an oscillator having a first signal and a second signal from first and second terminals, respectively, each of said first and second signals having an operating point potential that is different than the other and [each of] said first [and second signals] signal being input to both said first and second differential amplifier circuits and said second signal being input to both said first and second differential amplifier circuits to generate differential amplification outputs based on said first and second signals;

wherein the differential amplification outputs of said first and second differential amplification circuits are combined to provide an output.

8. (Amended) An oscillation circuit, comprising:

an oscillator having a first signal and a second signal from first and second terminals, respectively, each of said first and second signals having an operating point potential

that is different than the other and said first signal being input to both said first and second differential amplifier circuits and said second signal being input to both said first and second differential amplifier circuits to generate differential amplification outputs based on said first and second signals;

a first MOS transistor of a first conductivity type having a source, a drain and a gate, and receiving said first signal at the gate thereof;

a second MOS transistor of the first conductivity type having a source, a drain and a gate, and receiving said second signal at the gate thereof;

a first current mirror circuit comprising a third and a fourth MOS transistors of a second conductivity type each having a source, a drain and a gate, the drains of said third and fourth MOS [transistor] transistors being connected to the drains of said first and second MOS transistors, respectively, the gates of the third and fourth MOS transistors connected to each other and the gate and drain of said third MOS transistor;

a fifth MOS transistor of the second conductivity type having a source, a drain and a gate, and [receives] receiving the first signal at the gate thereof;

a sixth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the second signal at the gate thereof;

a second current mirror circuit comprising a seventh and an eighth MOS transistors of the first conductivity type each having a source, a drain and a gate, the drains of said seventh and eighth MOS transistors being connected to the drains of said fifth and sixth

MOS transistors, respectively, the gates of the seventh and eighth MOS transistors being connected to each other and the gate and drain of said seventh MOS transistor being connected; and

an output buffer circuit for generating an output signal based on a signal generated at the drain of said fourth MOS transistor and a signal generated at the drain of said eighth MOS transistor.